

实验室 电路

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连接/参考器件

ADF4002	鉴相器/PLL 频率合成器
AD9215-80	10 位、65 MSPS/80 MSPS/ 105 MSPS 、3 V ADC
HSC-ADC-EVALB-DCZ	评估板

使用 ADF4002 PLL 产生高速模数转换器所需的极低抖动编码（采样）时钟

电路功能与优势

本电路利用 ADF4002 频率合成器产生极低抖动编码（采样）时钟，以控制模数转换器 AD9215 的采样。编码时钟上的抖动会降低总信噪比 (SNR)，二者的关系如下式所示：

$$SNR = 20 \log_{10} \left(\frac{1}{2\pi f t_j} \right) \quad (1)$$

其中 f 为满量程模拟输入频率， t_j 为均方根抖动。公式 1 中的“SNR”是仅由时钟抖动决定的 SNR，与 ADC 的分辨率无关。

电路描述

ADF4002 由低噪声数字鉴频鉴相器 (PFD)、精密电荷泵、可编程参考分频器和可编程 N 分频器组成。14 位参考计数器 (R 计数器) 允许 PFD 输入端的 REFIN 频率为可选值。如果频率合成器与一个外部环路滤波器和电压控制振荡器 (VCO) 一起

使用，则可以实现完整的锁相环 (PLL)。

图 1 显示 ADF4002 与 VCXO 共同为高速模数转换器提供编码时钟。本应用中的转换器为一款 10 位转换器 AD9215-80，它可接受最高 80 MHz 的编码时钟。为实现稳定的低抖动时钟，采用 77.76 MHz 窄带 VCXO。本例假设参考时钟为 19.44 MHz，为了将 ADF4002 的相位噪声贡献降至最低，采用最小的倍增系数 4。因此，R 分频器编程设置为 1，N 分频器编程设置为 4。ADF4002 的电荷泵输出（引脚 2）驱动环路滤波器，环路滤波器的带宽经过优化，以提供最佳的均方根抖动，它是决定 ADC 信噪比的关键因素。如果带宽过窄，在相对于载波频率的频偏较小处，VCXO 噪声占主导地位。如果带宽过宽，ADF4002 噪声将在 VCXO 噪声低于 ADF4002 噪声情况下的频偏处占主导地位。因此，环路滤波器的最佳带宽对应 VCXO 噪声与 ADF4002 带内噪声的交点。

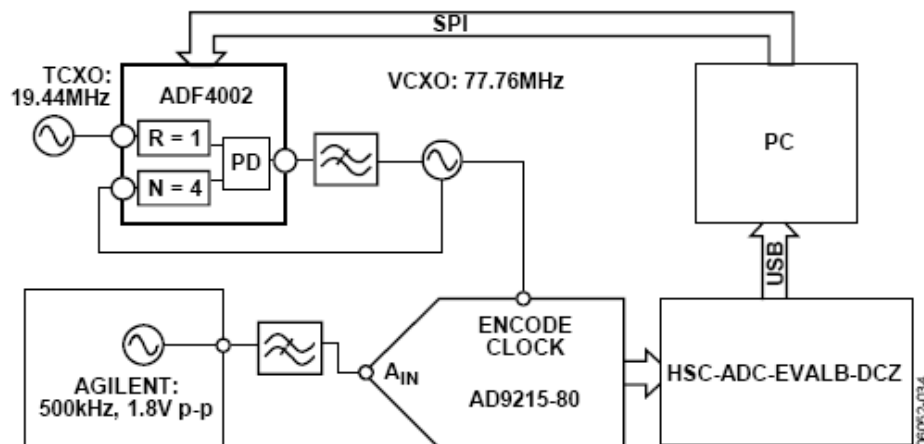


图 1. ADF4002 用作高速 ADC 的编码（采样）时钟

Rev.A

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可以使用ADIsimPLL™设计工具(3.0 版)来设计环路滤波器,该工具可从analog.com/pll免费下载。测量所得的均方根抖动小于 1.2 ps,假设输入信号为 20 MHz,利用上述公式 1 可得出SNR理论值(仅由抖动决定)为 76.4 dB。该值比ADC的额定SNR (59 dB)高出 17.4 dB,导致总SNR仅降低 0.1 dB。如果均方根抖动提高至 6 ps,则 20 MHz时由抖动决定的相应SNR为 62.4 dB,导致总SNR为 57.4 dB。

为进行精确测量,需要低噪声、低失真模拟输入源。利用优质信号发生器及后置调谐至目标频率的带通滤波器即可实现。虽然图 1所示采用 500 kHz信号源,但是应能够测试更高频率的信号源。每种附加频率均需要一个独立的带通滤波器。

图 1 所示设置使用ADF4002、AD9215和

HSC-ADC-EVALB-DCZ,用户可以快速有效地确定转换器和编码时钟是否合适。SPI接口用来控制ADF4002,USB接口帮助控制AD9215-80的操作。控制器板将FFT信息送回PC,如果PC使用ADI公司的ADC Analyzer™软件,则会提供来自ADC的所有转换结果。为了达到所需的性能,整个系统必须使用出色的布局、接地和去耦技术。

常见变化

基于PLL的时钟产生电路,如图 1所示,经常用于从高噪声系统时钟产生干净的低抖动时钟。ADI公司提供许多不同的频率合成和时钟产生产品,均适合类似的应用。欲了解更多信息,请参考analog.com/clock-timing。

进一步阅读

[ADIsimPLL Phase-Locked Loop Circuit Design Software.](#)

[HSC-ADC-EVALB-DCZ High Speed ADC Data Capture Kit.](#)

[Kester, Walt. 2005. *The Data Conversion Handbook*. Analog Devices. Chapters 6 and 7.](#)

[Kester, Walt. 2006. *High Speed System Applications*. Analog Devices. Chapter 2, "Optimizing Data Converter Interfaces,"](#)

[Kester, Walt. 2006. *High Speed System Applications*. Analog Devices. Chapter 3, "DACs, DDSs, PLLs, and Clock Distribution."](#)

[MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.](#)

[MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.](#)

数据手册和评估板

[AD9215 Data Sheet.](#)

[ADF4002 Data Sheet.](#)

[HSC-ADC-EVALB-DCZ Evaluation Board.](#)

修订历史

5/09—Rev. 0 to Rev. A

Updated Format Universal

10/08—Revision 0: Initial Version

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